

# ISL70244SEH Evaluation Board User's Guide

## Introduction

The ISL70244SEHEV1Z evaluation platform is designed to evaluate the ISL70244SEH. The ISL70244SEH contains two high speed and low power op amps designed to take advantage of its full dynamic input and output voltage range with rail-to-rail operation. By offering low power, low offset voltage, and low temperature drift coupled with its high bandwidth and enhanced slew rates upwards of 50V/μs, these op amps make it ideal for applications requiring both high DC accuracy and AC performance. These amplifiers are designed to operate over a single supply range of 2.7V to 40V or a split supply voltage range of ±1.35V to ±20V. The ISL70244SEH is manufactured in Intersil's PR40, silicon on insulator (SOI) process, which makes this device immune to Single Event Latch-up and provides excellent radiation tolerance. This makes it the ideal choice for high reliability applications in harsh radiation-prone environments.

## Reference Documents

- [ISL70244SEH Datasheet](#)
- ISL70244SEH SMD [5962-13248](#)
- ISL70244SEH Radiation Test Report

## Evaluation Board Key Features

- Single Supply Operation: +3V to +40V
- Dual Supply Operation: +1.8V/-1.2V to ±20V
- Singled-Ended or Differential Input Operation
- External VREF Input
- Banana Jack Connectors for Power Supply and VREF Inputs
- BNC Connectors for Op Amp Input and Output Terminals
- Convenient PCB Pads for Op Amp Input/Output Impedance loading.

## Power Supplies

External power connections are made through the +V, -V, VREF and Ground connections on the evaluation board. For single supply operation, the -V and Ground pins are tied together to the power supply negative terminal. For split supplies, +V and -V terminals connect to their respective power supply terminals. De-coupling capacitors C2, C3, C4 and C6 connect to their respective supplies through R11 and R15 resistors. These resistors are 100Ω but can be changed by the user to provide additional power supply filtering, or to reduce the voltage rate-of-rise to less than ±1V/μs. Two additional capacitors, C5 and C7, are connected close to the part to filter out high frequency noise. Anti-reverse diode D1 protects the circuit in the momentary case of accidentally reversing the power supplies to the evaluation board. The VREF pin can be connected to ground to establish a ground referenced input for split supply operation, or can be externally set to any reference level for single supply operation.

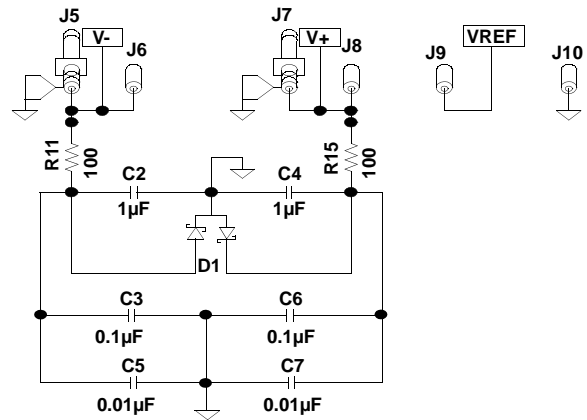


FIGURE 1. POWER SUPPLY CIRCUIT

## Amplifier Configuration

A simplified schematic of the evaluation board is shown in Figure 2. The input stage with the components supplied is shown in Figure 3, with a closed loop gain of 10V/V. The differential amplifier gain is expressed in Equation 1:

$$V_{OUT} = (V_{IN+} - V_{IN-}) \cdot (R_F / R_{IN}) + V_{REF} \quad (EQ. 1)$$

For single-ended input with an inverting gain  $G = -10V/V$ , the  $IN+$  input is grounded and the signal is supplied to the  $IN-$  input.  $VREF$  can be connected to a reference voltage between the  $V+$  and  $V-$  supply rails. For non-inverting operation with  $G = 11V/V$ , the  $IN-$  input is grounded and the signal is supplied to the  $IN+$  input. The non-inverting gain is strongly dependent on any resistance from  $IN-$  to GND. For good gain accuracy, a 0Ω resistor should be installed on the empty R5 pad. The  $VREF$  pin must be connected to ground to establish a ground referenced input for dual supply operation, or can be externally set to any reference level for single supply operation.  $VREF$  should not be left floating.

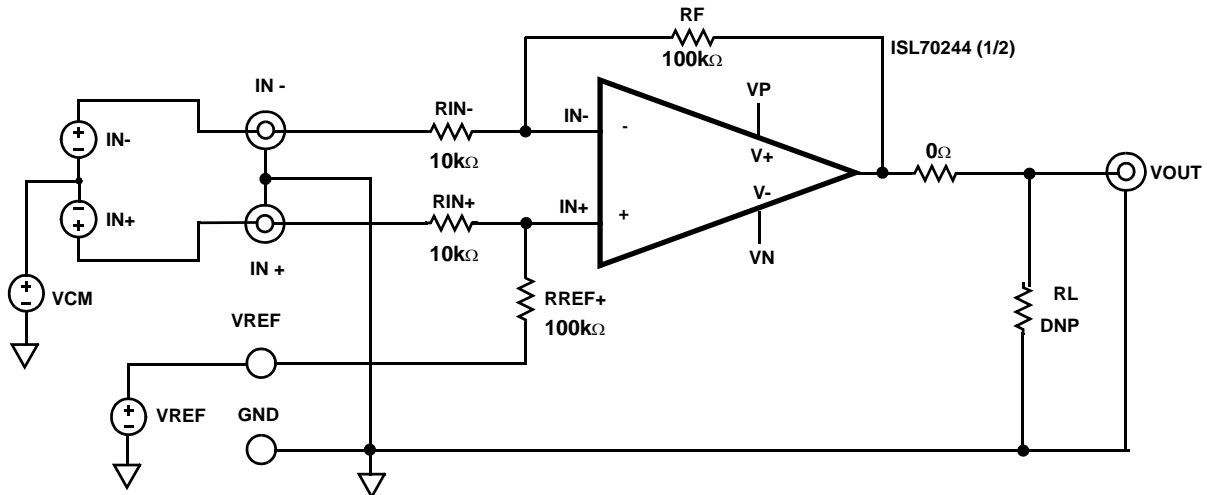


FIGURE 2. BASIC AMPLIFIER CONFIGURATION

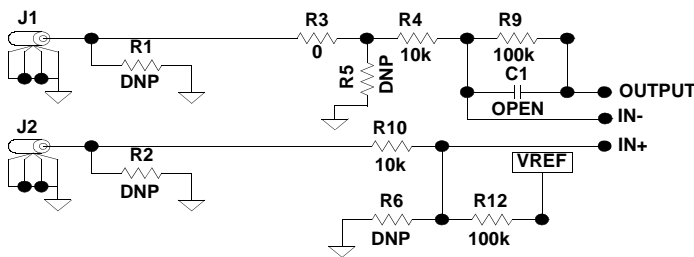


FIGURE 3. INPUT STAGE (1/2)

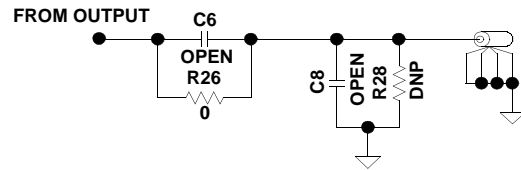


FIGURE 4. OUTPUT STAGE (1/2)

## User-selectable Options

Component pads are included to enable a variety of user-selectable circuits to be added to the amplifier VREF, inputs, outputs, and the amplifier feedback loops.

A voltage divider (Figure 3, R6 and R12) can be added to establish a power supply-tracking common mode reference using the VREF input. The input stages (see Figure 3) have additional resistor and/or capacitor pads that maybe used to add voltage divider networks or feedback networks for adding input attenuation, or to establish input DC offsets through the VREF pin. The output stages (see Figure 4) have additional resistor and capacitor placements for loading.

**NOTE:** Operational amplifiers are sensitive to output capacitance and may oscillate. In the event of oscillation, reduce output capacitance by using shorter cables, or add a resistor in series with the output.

# Application Note 1888

TABLE 1. ISL70244SEHEV1Z COMPONENTS PARTS LIST

DEVICE #	DESCRIPTION	COMMENTS
C2, C4	CAP, SMD, 1210, 1 $\mu$ F, 50V, 10%, X7R, ROHS	Power Supply Decoupling
C3, C6	CAP, SMD, 0805, 0.1 $\mu$ F, 50V, 10%, X7R, ROHS	Power Supply Decoupling
C5, C7	CAP, SMD, 0603, 0.01 $\mu$ F, 50V, 10%, X7R, ROHS	Power Supply Decoupling
C1, C8-C12	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS	User selectable capacitors - not populated
D1	DIODE-RECTIFIER, SMD, SOD-123, 2P, 40V, 0.5A, ROHS	Reverse Power Protection
U1	ISL70244SEH, DUAL OP-AMP, 10Ld. FLATPACK	
R1, R2, R5-R8, R14, R20, R23, R24,	RESISTOR, SMD, 0603, 0.1%, MF, DNP-PLACE HOLDER	User selectable resistors - not populated
R3, R20-R22	RES, SMD, 0603, 0 $\Omega$ , 1/10W,TF, ROHS	Zero ohm user selectable resistors
R4, R10, R17, R18	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	Gain resistors
R10, R12, R13, R16	RES, SMD, 0603, 100k, 1/10W, 1%, TF, ROHS	Gain resistors

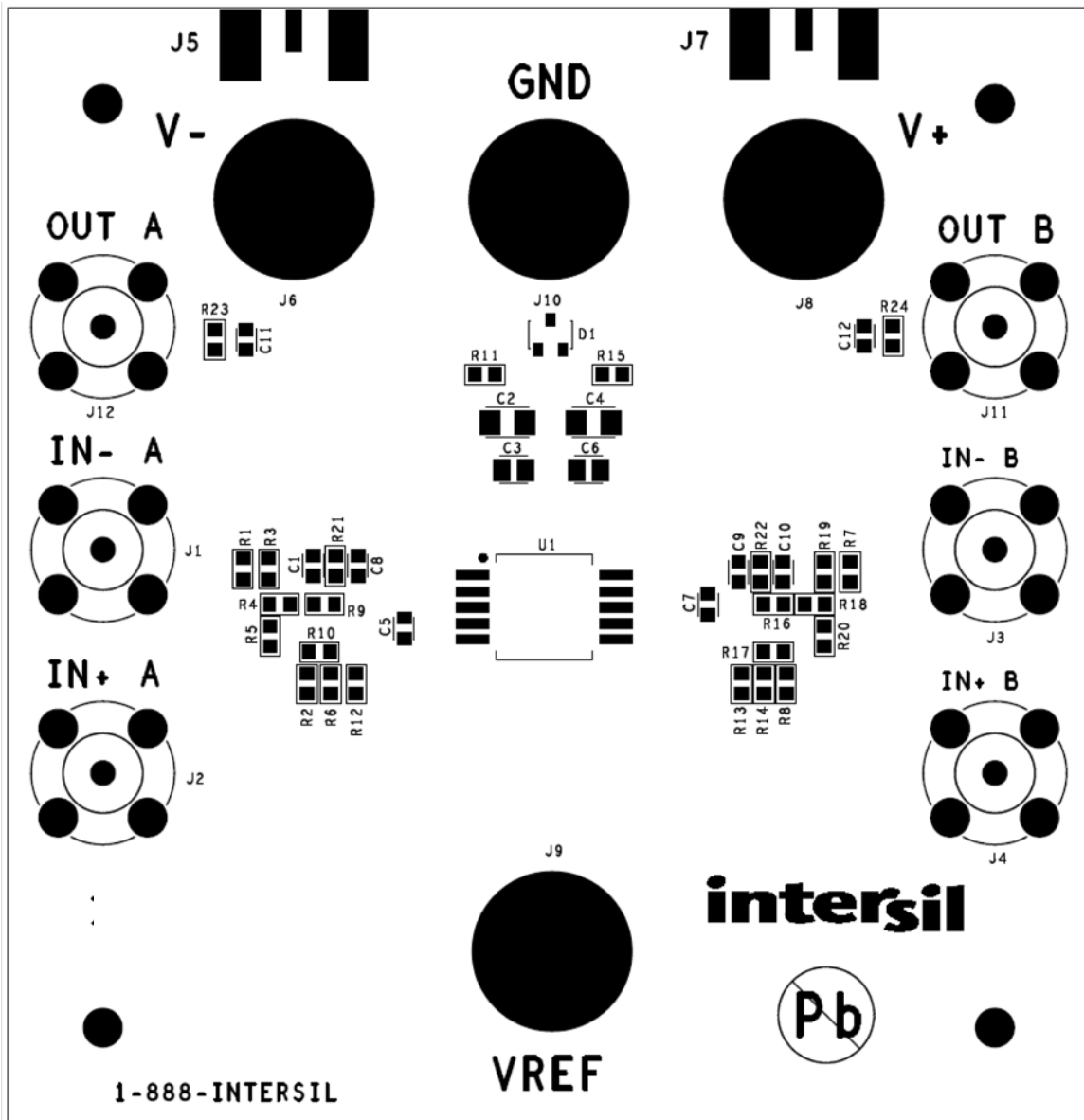


FIGURE 5. ISL70244SEHEV1Z TOP VIEW

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)

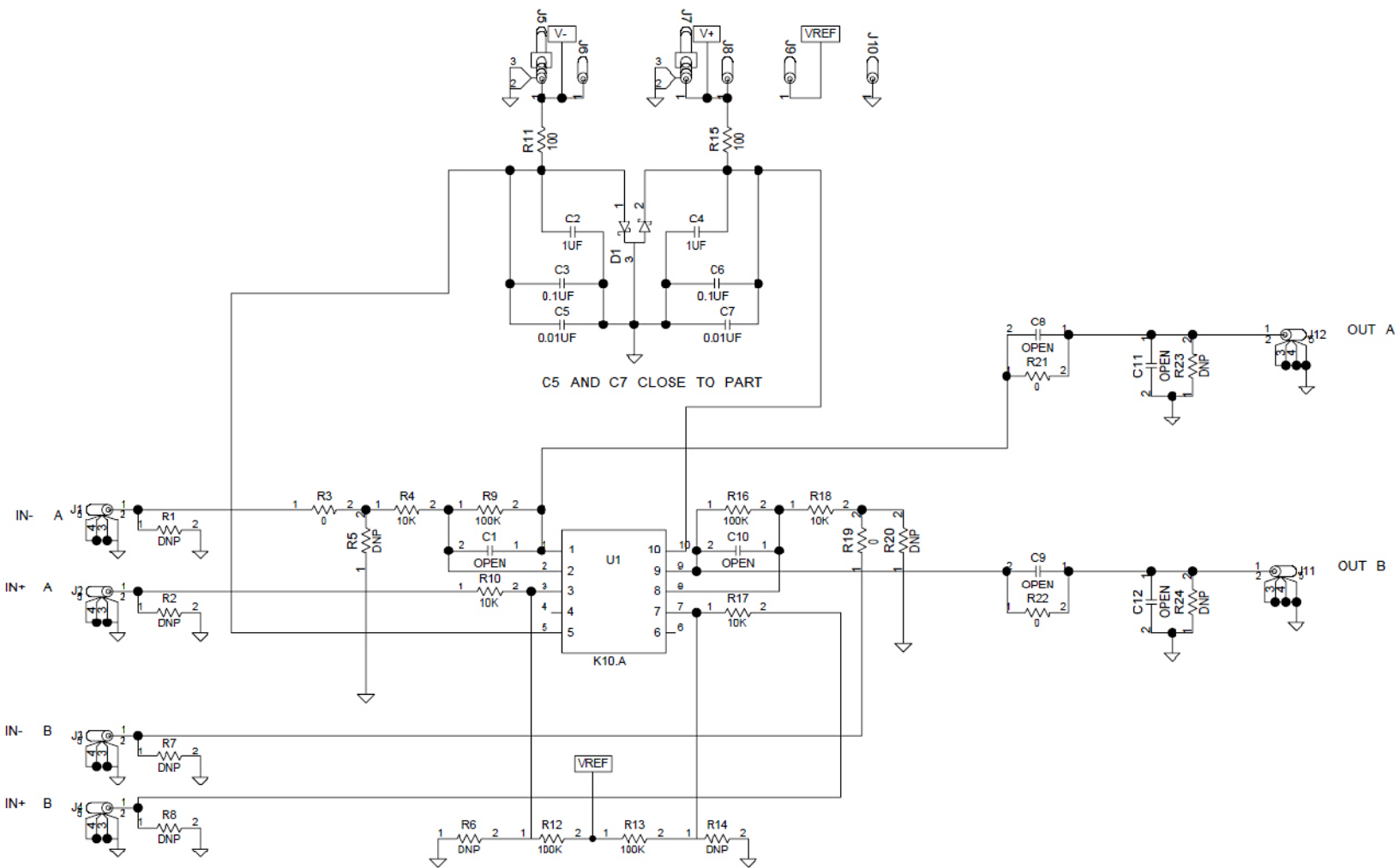


FIGURE 6. ISL70244SEHEV1Z SCHEMATIC DIAGRAM